## REMARKS

Reconsideration of this application as amended is respectfully requested. No new matter has been added. Claims 1-36 remain pending. The remarks below in connection with the claim rejections refer to the claims as amended herein.

***Claim Rejections - 35 U.S.C. § 102***

Claims 1-3, 5-7, 9-11, 13-36 have been rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,442,644[1] to Gustavson et al. ("Gustavson").

Claim 1 recites, in part:

> a first data bus connected to the first memory controller and to the first memory component, wherein the first data bus uses differential signaling and has a first data bus symbol time that is shorter than a first address and control bus symbol time of the first address and control bus.

Gustavson discloses a Synchronous-Link Dynamic Random Access Memory (SLDRAM) System comprising CommandLink (151) for transferring command and address words in synchronization with command clock signals (Gustavson col. 8 lines 32-47), and DataLink_A (155) for transferring data words in synchronization with data clock signals (Gustavson, col. 9 lines 20-49), and that the data clock signals and the command clock signals operate at the *same frequency* (Gustavson, lines 40-52). Nowhere does Gustavson disclose or suggest a first data bus having "a first data bus symbol time *that is shorter* than a first address and control bus symbol time of the first address and control bus," as recited in claim 1. Applicant therefore submits that Gustavson does not anticipate claim 1 nor dependent claims 2, 3, and 30.

Claim 5 recites, in part:

> a first data bus connected to the first memory controller and to the first memory component, wherein the first data bus has a first data bus symbol time that is shorter than a first address and control bus symbol time of the first address and

control bus and wherein the first address and control bus symbol time is shorter than a first clock signal cycle time of the first clock signal.

Applicant submits that, for at least the reasons discussed above in reference to claim 1, Gustavson does not disclose the above-recited limitation of claim 5 and therefore does not anticipate claim 5 nor dependent claims 6, 7, and 31.

Claim 9 recites, in part:

a first data bus connected to the first memory controller and to the first memory component, wherein the first memory component includes a first termination structure connected to the first data bus and wherein the first data bus has a first data bus symbol time that is shorter than a first address and control symbol time of the first address and control bus.

Applicant submits that, for at least the reasons discussed above in reference to claim 1, Gustavson does not disclose the above-recited limitation of claim 9 and therefore does not anticipate claim 9 nor dependent claims 10, 11, 13, and 32.

Claim 14 recites, in part:

a first data bus connected to the first memory controller and to the first memory component, wherein the first memory component includes a first termination structure connected to the first data bus, wherein the first data bus uses differential signaling, and wherein the first address and control bus does not use differential signaling.

Gustavson discloses a plurality of SLDRAM Modules (110-180) each coupled to DataLink_A (155), and wherein DataLink_A comprises a single-end terminated transmission line having a termination resistor ($R_T$) at the far end of the line (Gustavson, Fig. 1B, col. 14 lines 52-59). However, nowhere does Gustavson disclose a first memory component, "wherein *the first memory component includes a first termination structure*

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1 The Examiner has confirmed, via telephone, that the patent number was improperly cited in the Office Action (originally US 5,778,419 to Hansen et al.), and should in fact be US 6,442,644 to Gustavson et al.

connected to the first data bus," as recited in claim 14. Applicant therefore submits that Gustavson does not anticipate claim 14 nor dependent claims 15-17 and 33.

Claim 18 recites, in part:

> a first data bus connected to the first memory controller and to the first memory component, wherein the first data bus uses differential signaling and wherein the first memory component accesses a first word stored in the first memory component, the first word being wider than a first data bus width of the first data bus.

In the embodiment disclosed by Gustavson, DataLink_A comprises eighteen single-end terminated transmission lines (DQ(0:17)_A) for transmitting a data word from a SLDRAM module (110), wherein the data word is 18-bits wide (Gustavson, col. 9 lines 20-37). Nowhere does Gustavson disclose or suggest a first memory component that "accesses a first word stored in the first memory component, the first word being *wider* than a first data bus width of the first data bus," as recited in claim 18. Applicant therefore submits that Gustavson does not anticipate claim 18 nor dependent claims 19, 20, and 34.

Claim 21 recites, in part:

> a first data bus connected to the first memory controller and to the first memory component, wherein the first memory controller includes a first receive circuit having a first read timing adjustment subcircuit for adjusting a first adjustable read data sampling time point for first read data sampled from the first data bus and wherein the first data bus uses differential signaling.

Gustavson discloses a Command Module (150) for transmitting command clock signals in synchronization with a predefined first synchronization sequence to be received by each of the SLDRAM Modules (110-180), each of which adjusts its own internal parameters so as to optimize local recognition of the predefined synchronization sequence in synchronism with the command clock signals (Gustavson, col. 11 line 60 to

col. 12 line 56). Thus, even assuming *arguendo* that the Command Module of Gustavson constitutes a first memory controller, Gustavson still does not disclose a first memory controller including "a first receive circuit having a first read timing adjustment subcircuit for adjusting a first adjustable read data sampling point for first read data sampled from the first data bus," but rather that each SLDRAM Module performs its own self-synchronizing operation in response to the first synchronization sequence *transmitted* by the Command Module. In view of this clear distinction, applicant submits that Gustavson does not anticipate claim 21 nor dependent claims 22-24 and 35.

Claim 25 recites, in part:

> a first data bus connected to the first memory controller and to the first memory component, wherein the first memory controller component includes a first receive circuit having a first read timing adjustment subcircuit for adjusting a first adjustable read data sampling time point for first read data sampled from the first data bus and wherein the first memory component includes a first termination structure connected to the first data bus.

Applicant submits that, for at least the reasons discussed above in reference to claim 21, Gustavson does not disclose the above-recited limitation of claim 25 and therefore does not anticipate claim 25 nor dependent claims 26-29 and 36.

***Allowable Subject Matter***

Claims 4, 8, and 12 have been objected to as being dependent upon a rejected base claim, but indicated to be allowable if rewritten in independent form to include all the limitations of the base claim and any intervening claims. Applicant acknowledges the allowability of claims 4, 8, and 12 if so amended, but respectfully declines to amend such claims at this time in view of the foregoing remarks.

***In Conclusion***

Applicant respectfully submits that all pending claims are in condition for allowance. If a telephone interview would be helpful in any way, the examiner is invited to call the undersigned attorney.

Authorization is hereby given to charge deposit account 501914 for any fee deficiency associated with this Amendment.

Respectfully submitted,

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